

FIG.1A

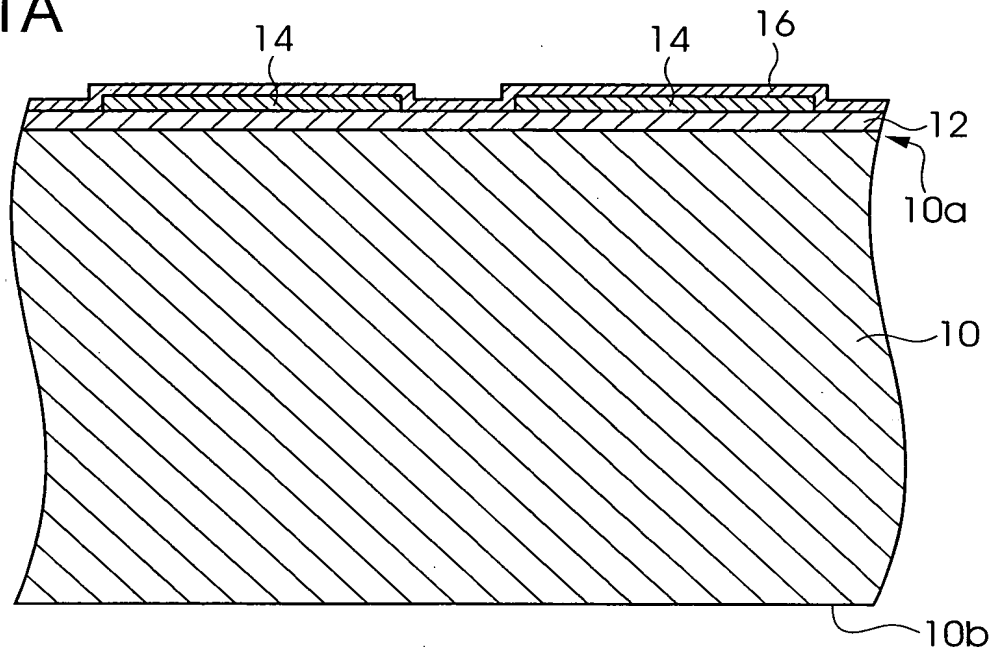


FIG.1B

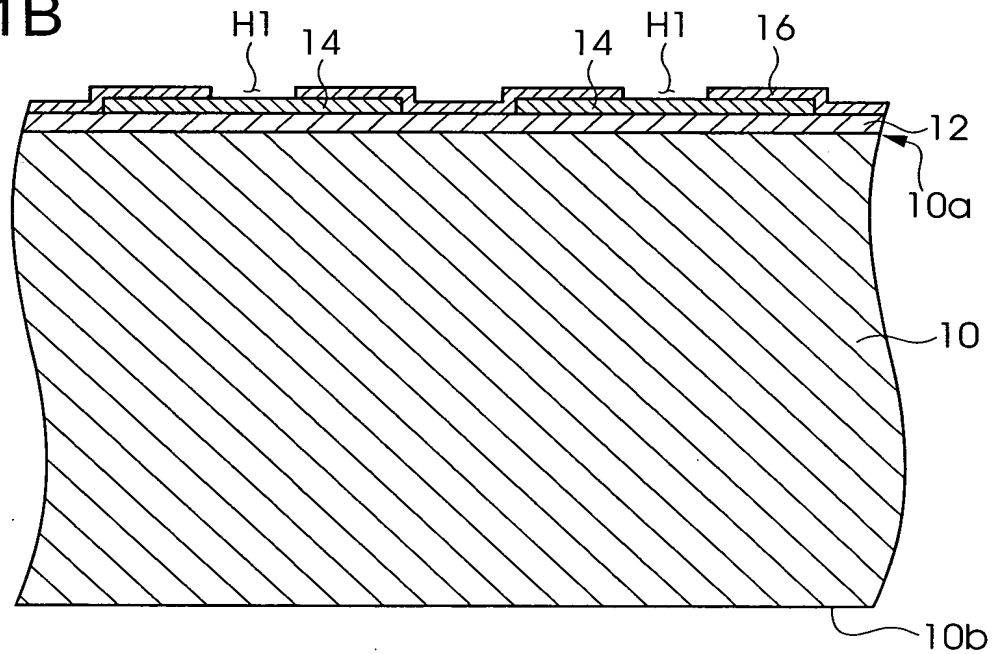


FIG.2A

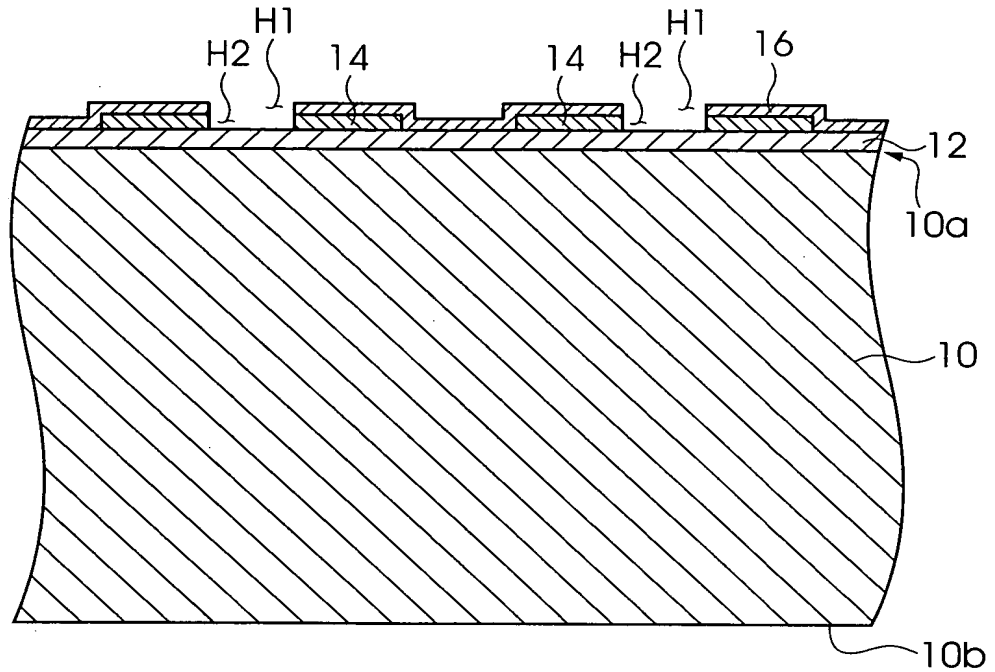


FIG.2B

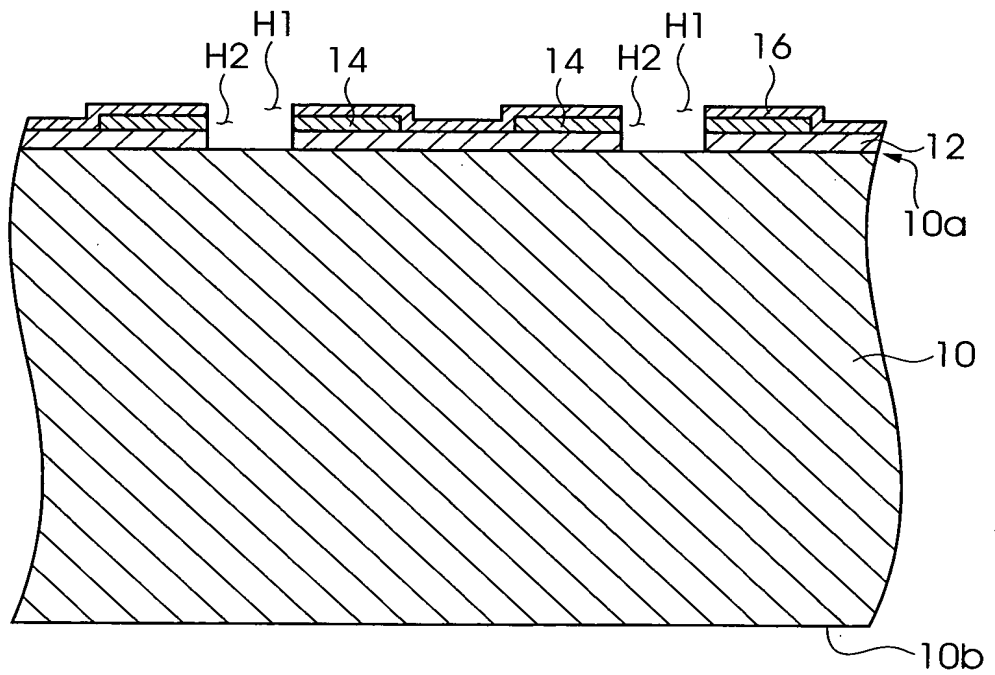


FIG.3A

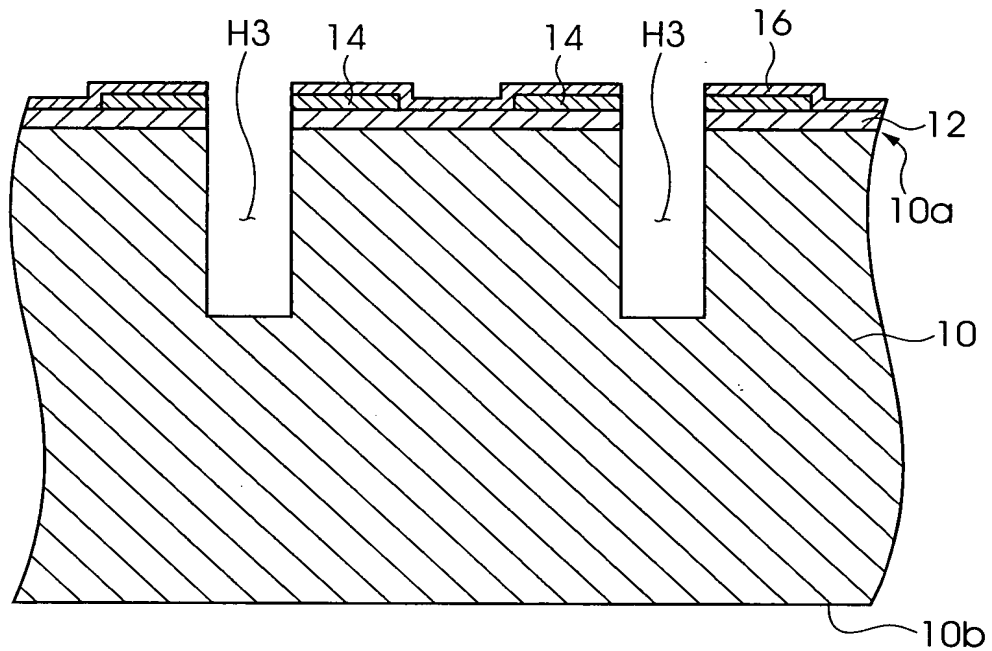


FIG.3B

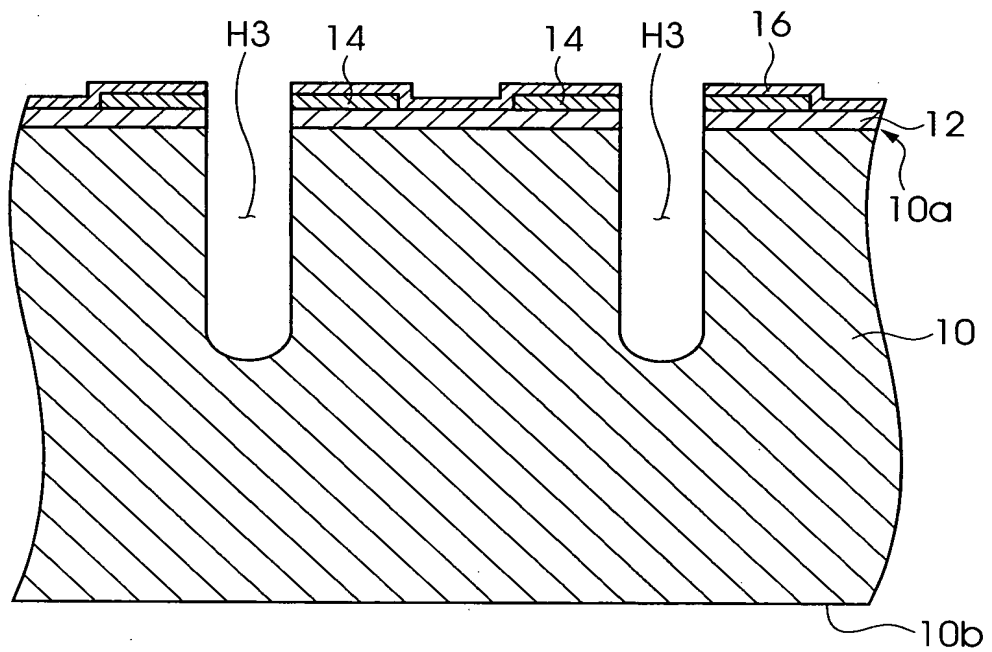


FIG.4A

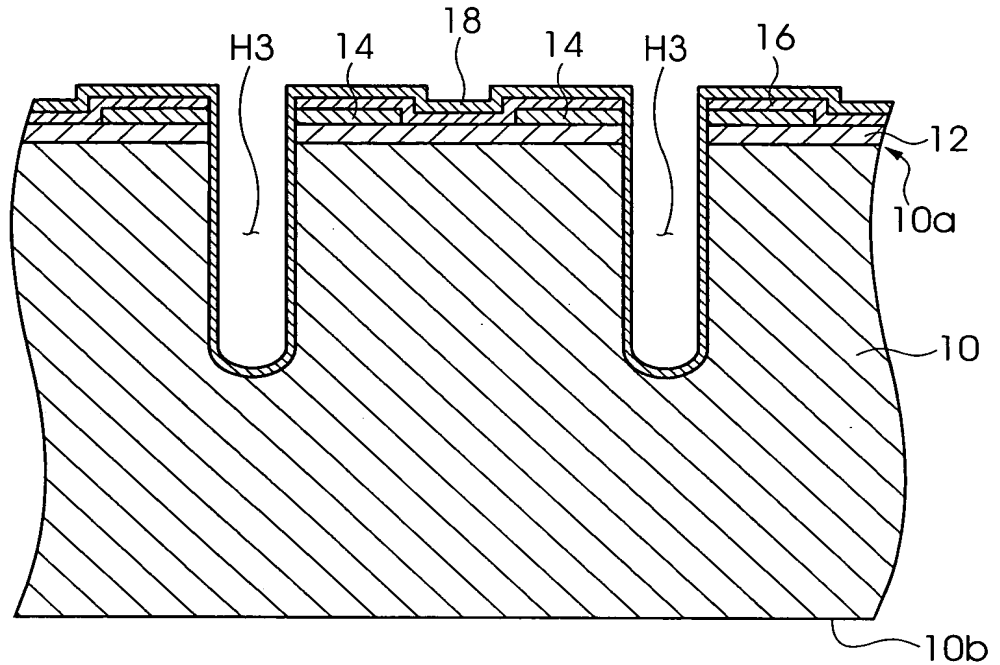
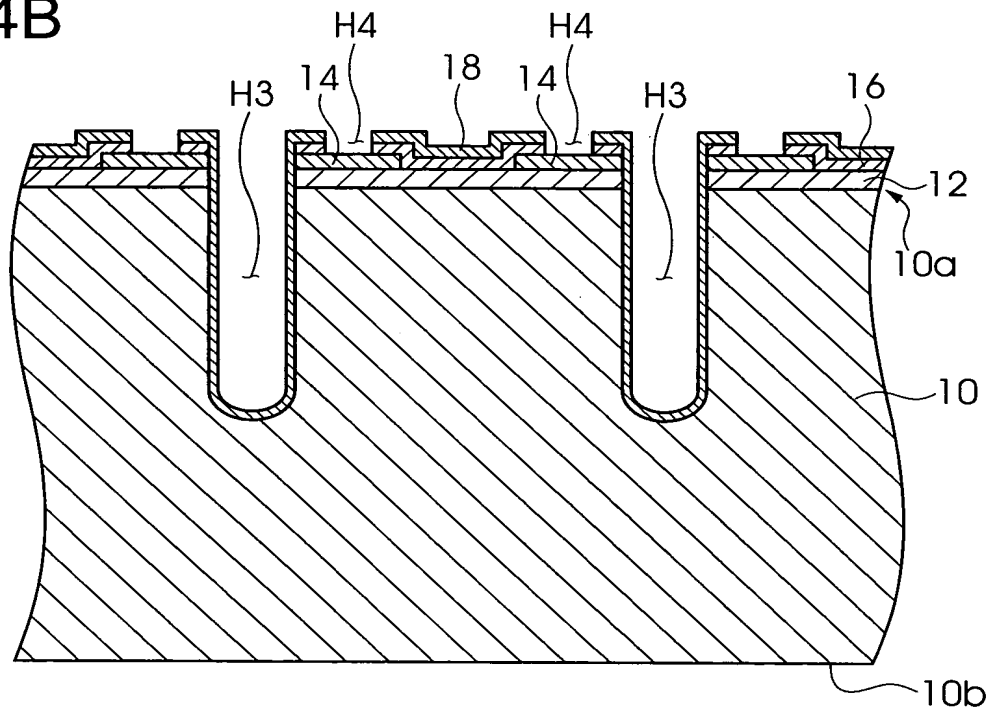


FIG.4B



[illegible]

This cross-sectional view shows a substrate 10 with two vertical pillars 18. Each pillar 18 is surrounded by a layer 20. The top of the device features a series of small, rectangular structures, possibly contacts or vias, arranged in a row across the top surface.

Figure 1C is a cross-sectional view of a semiconductor device. It shows a substrate 10 with a gate stack 18 and a gate electrode 20. The gate stack 18 is formed on the substrate 10, and the gate electrode 20 is formed on top of the gate stack 18. The gate stack 18 is divided into three regions by two vertical lines, and the gate electrode 20 is formed on top of each of these three regions.

FIG.6

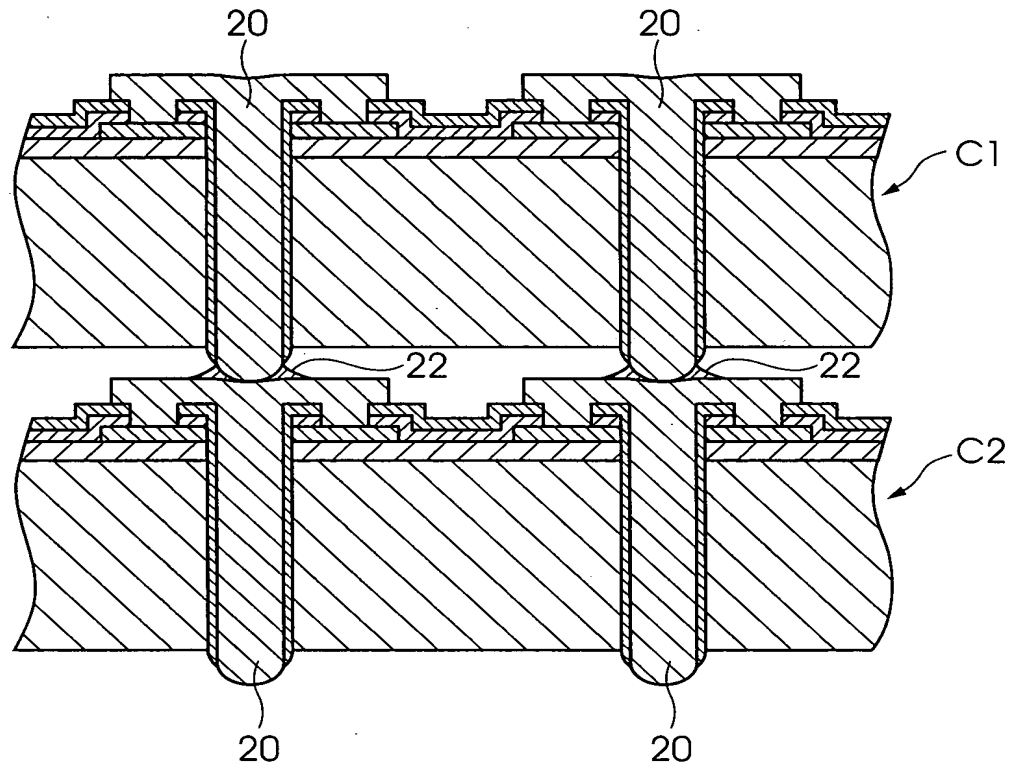


FIG.7A

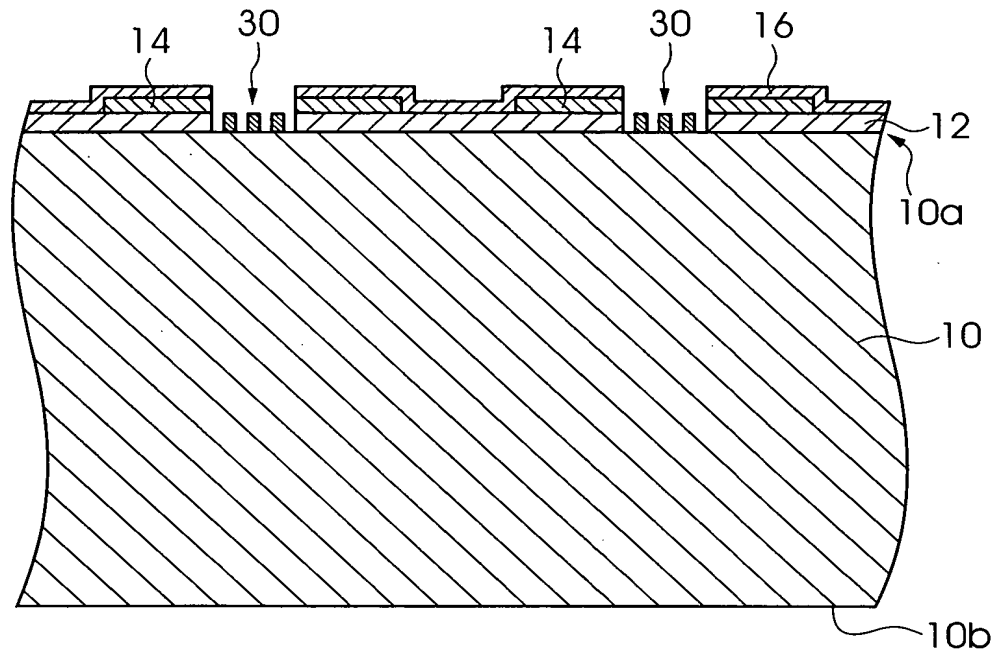


FIG.7B

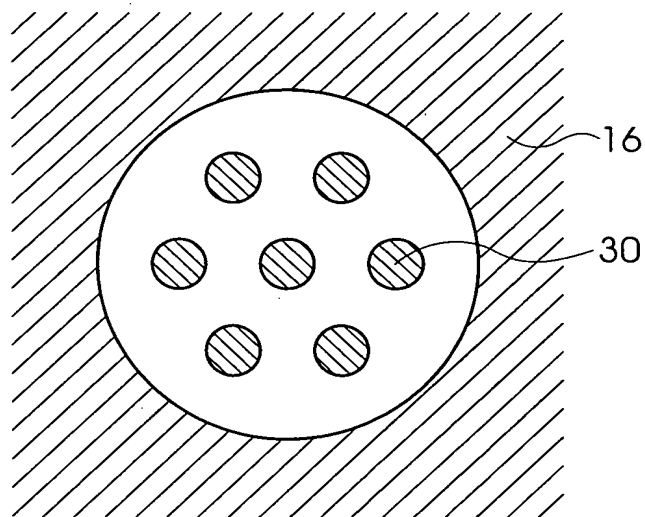


FIG.8A

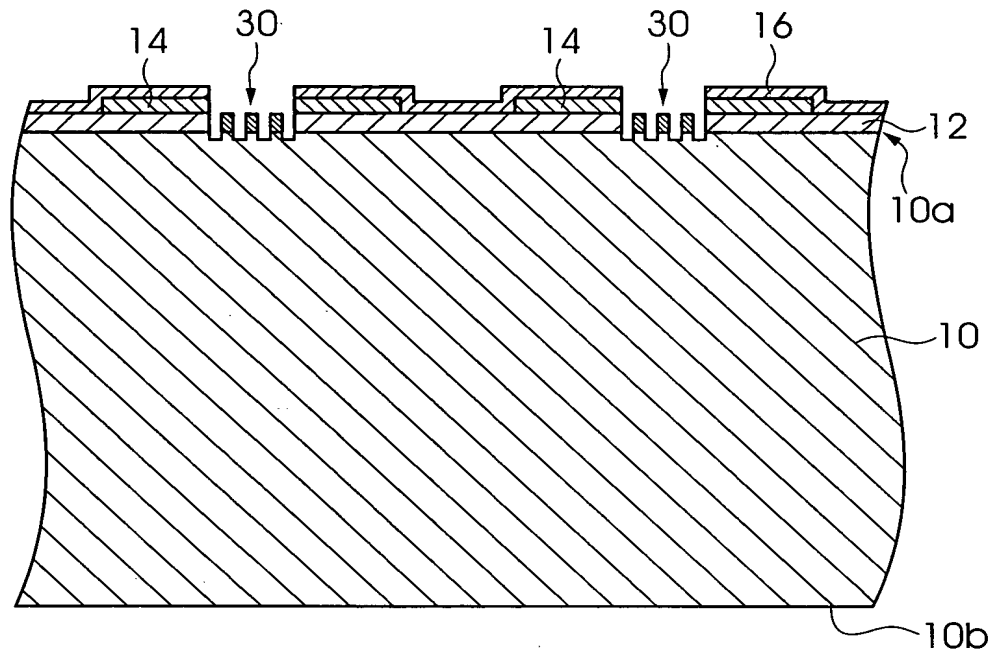


FIG.8B

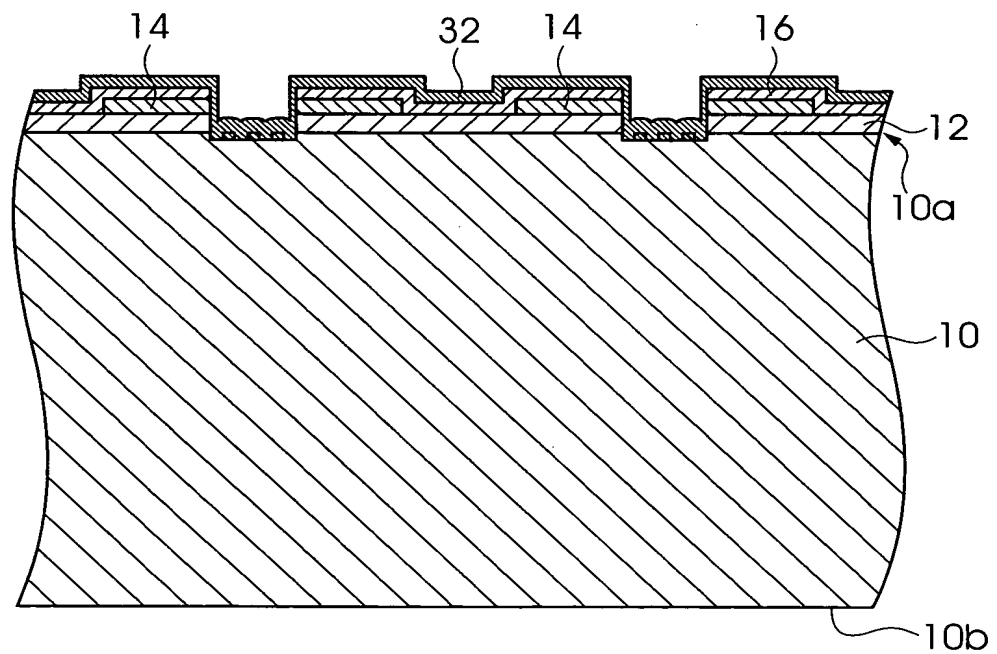




FIG.9A

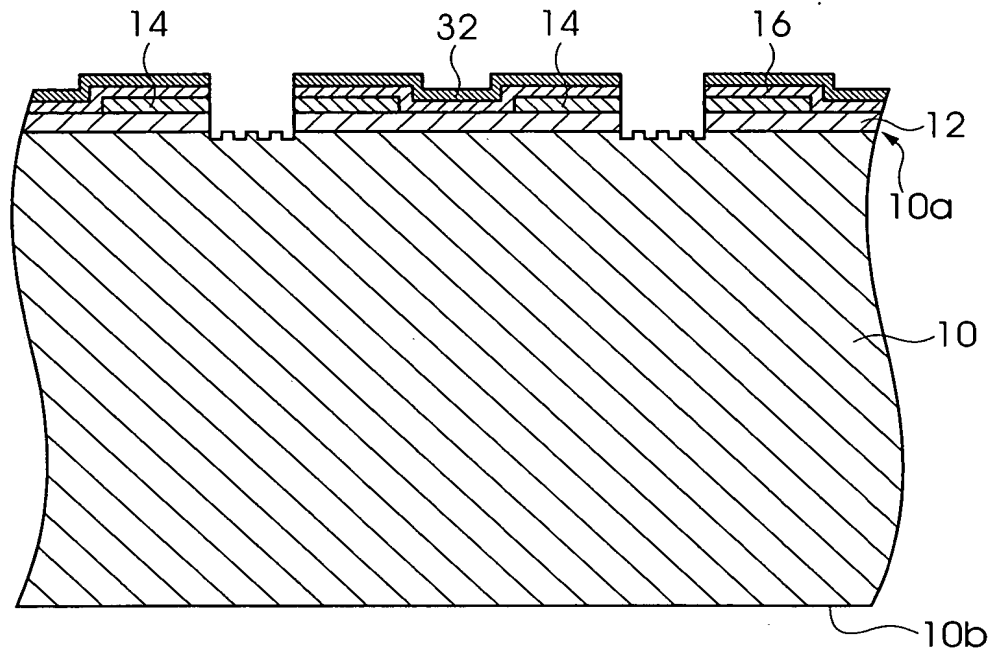


FIG.9B

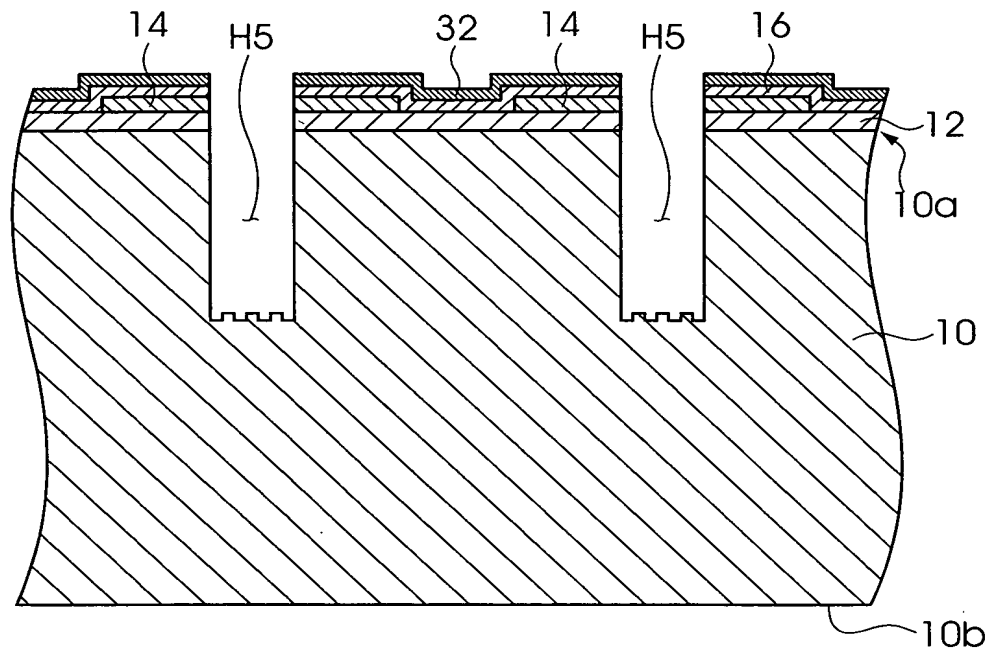




FIG.11A

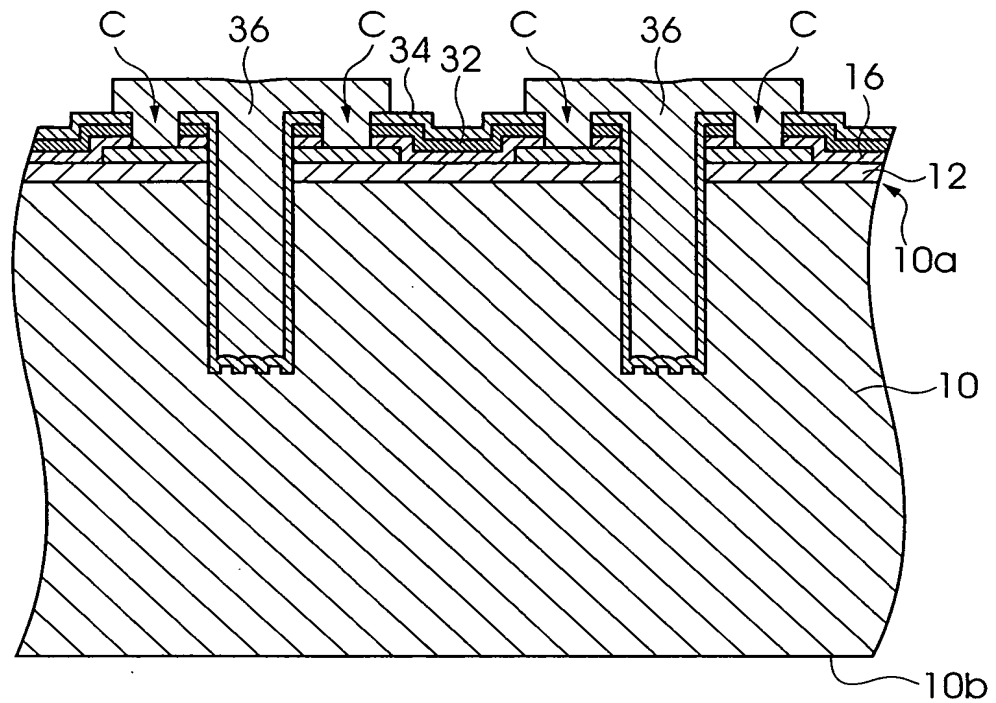


FIG.11B

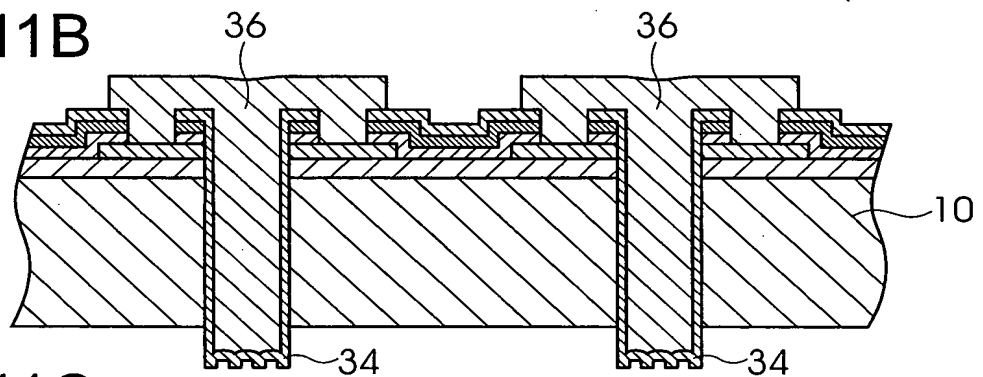


FIG.11C

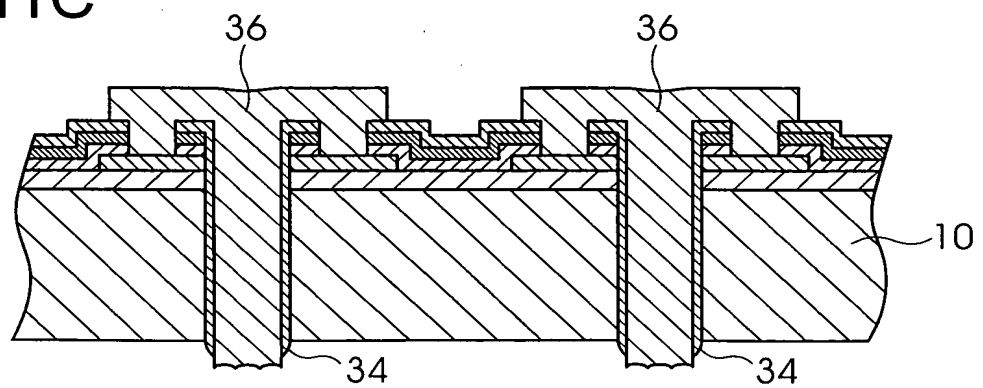
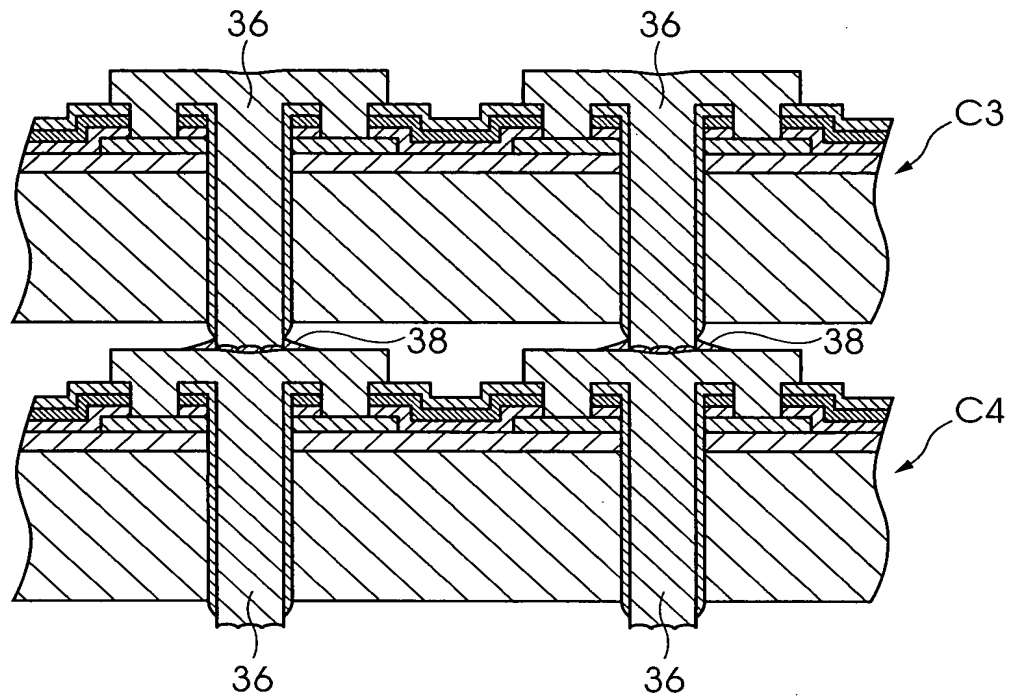


FIG.12



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FIG.13A

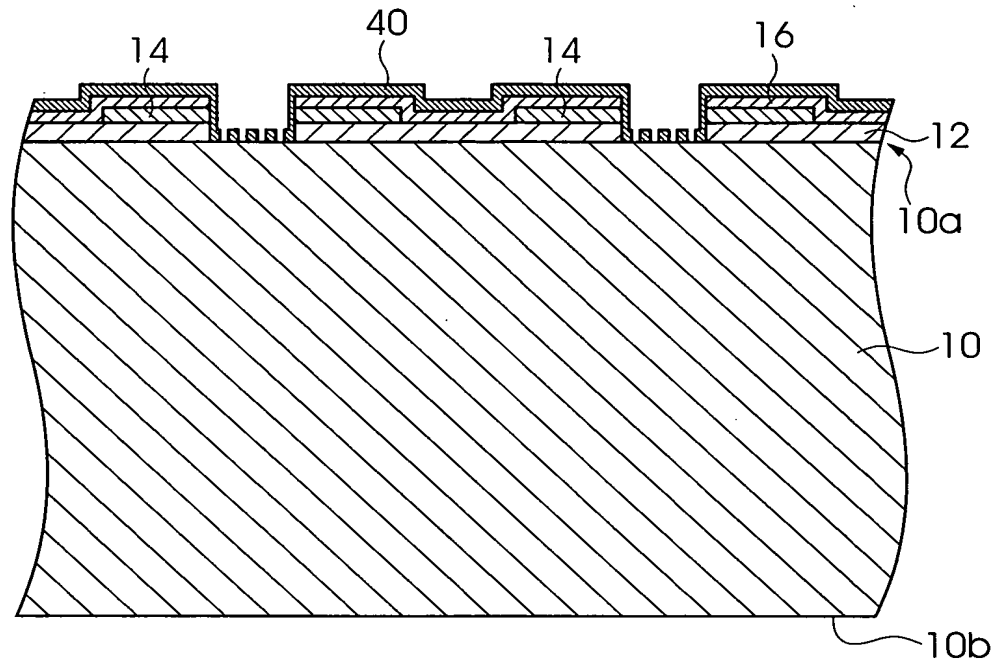
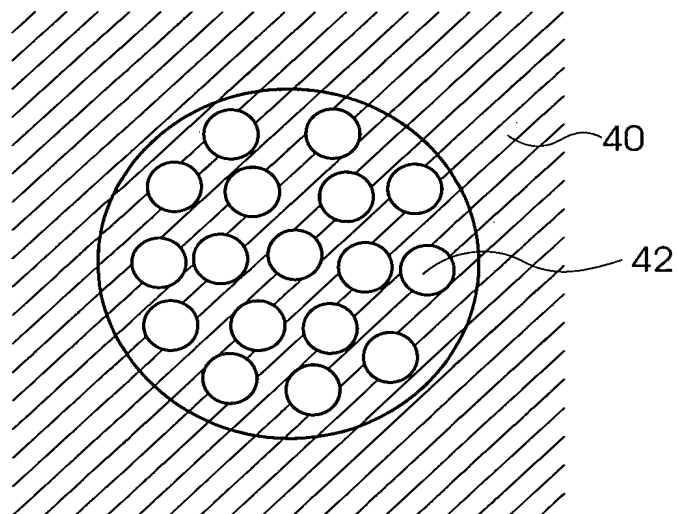


FIG.13B



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FIG.14A

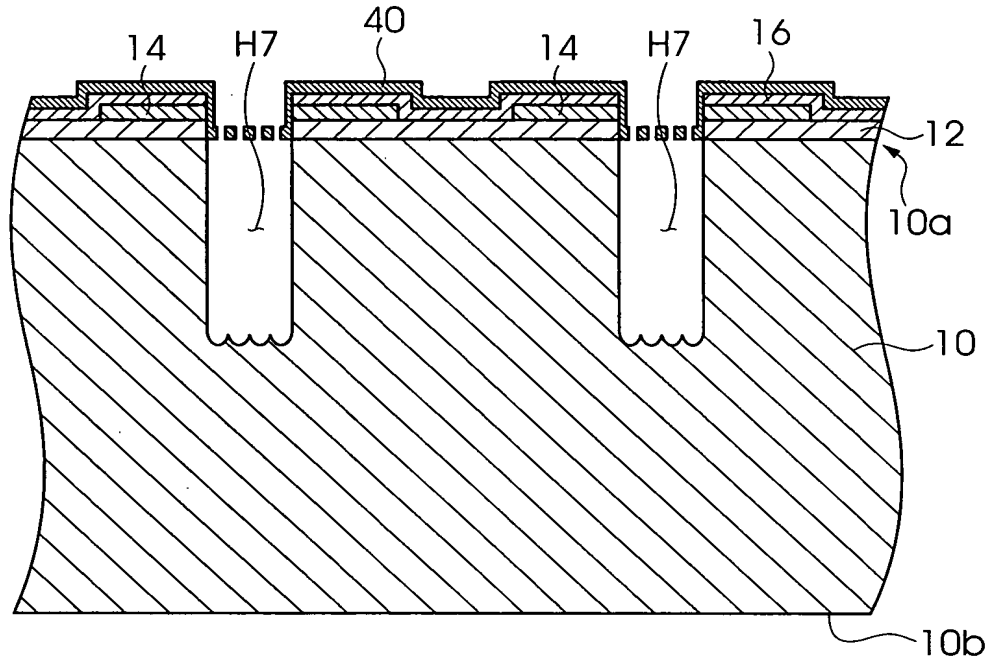


FIG.14B

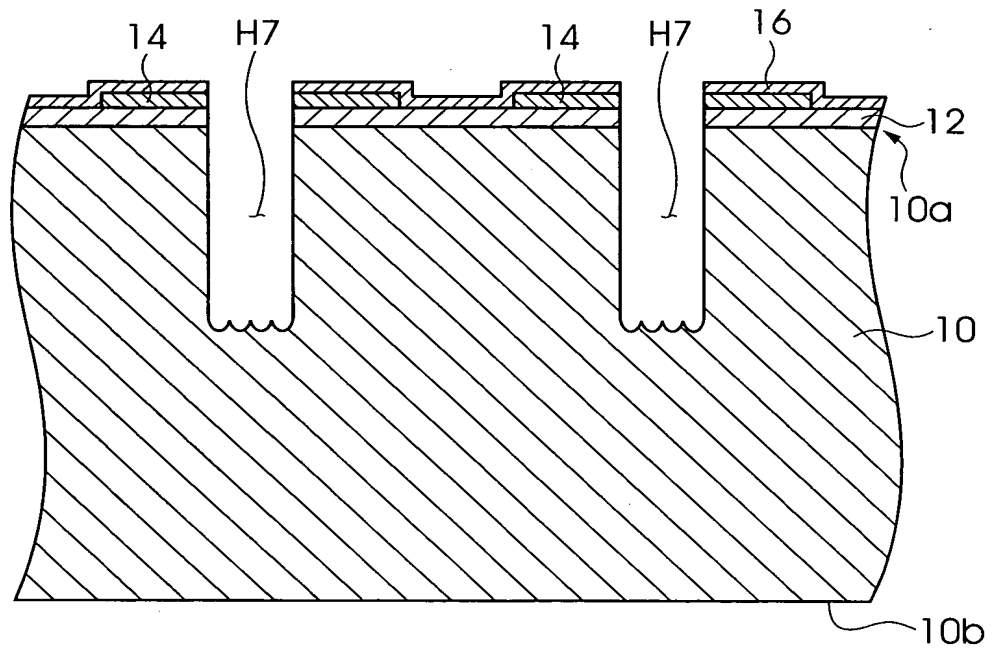


FIG.15A

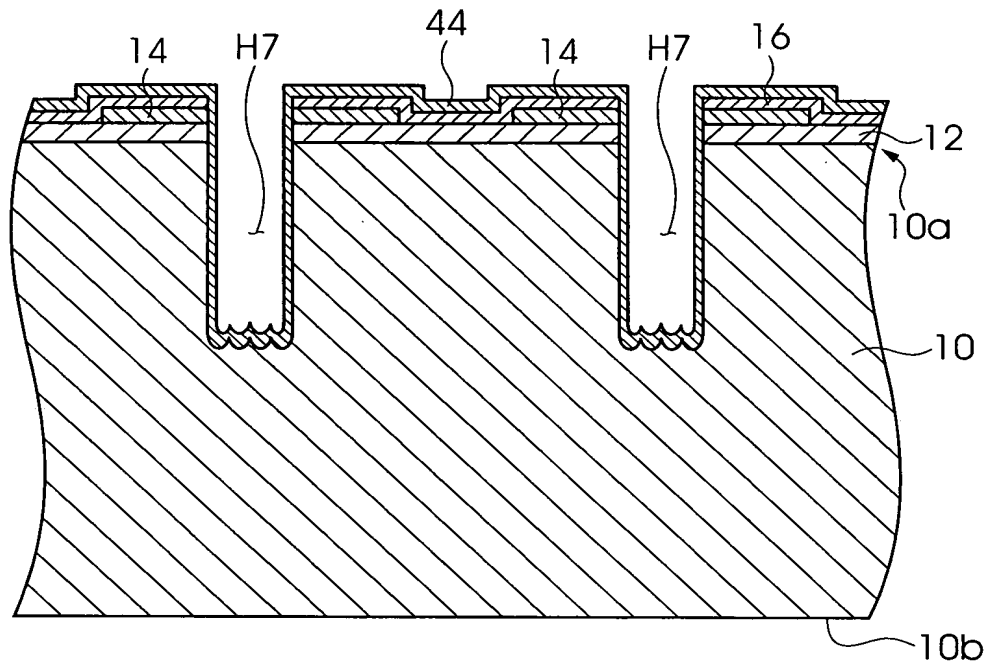
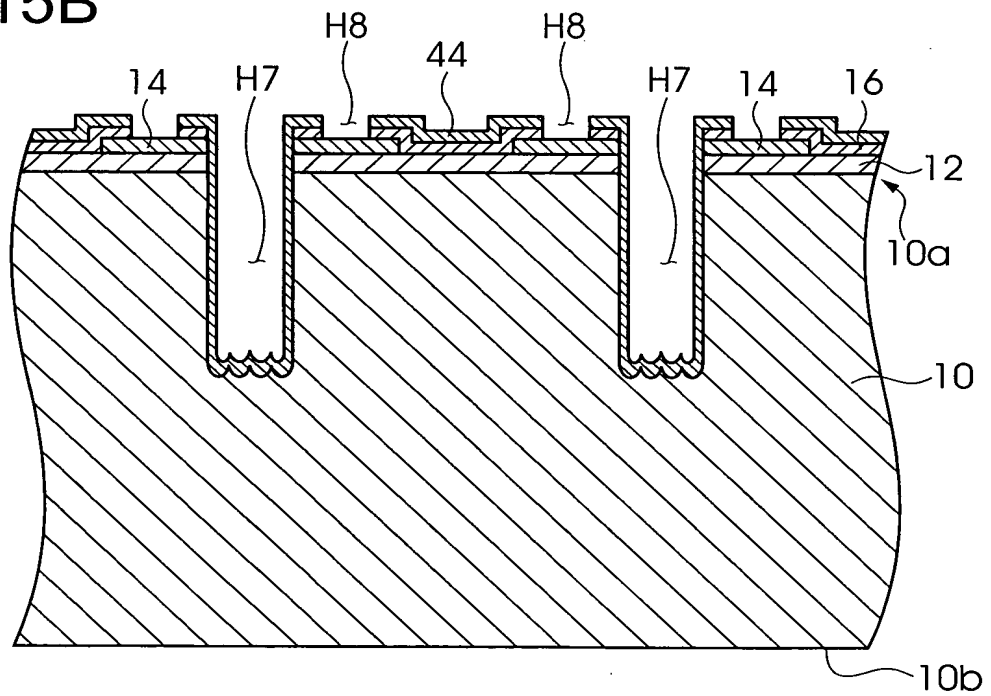
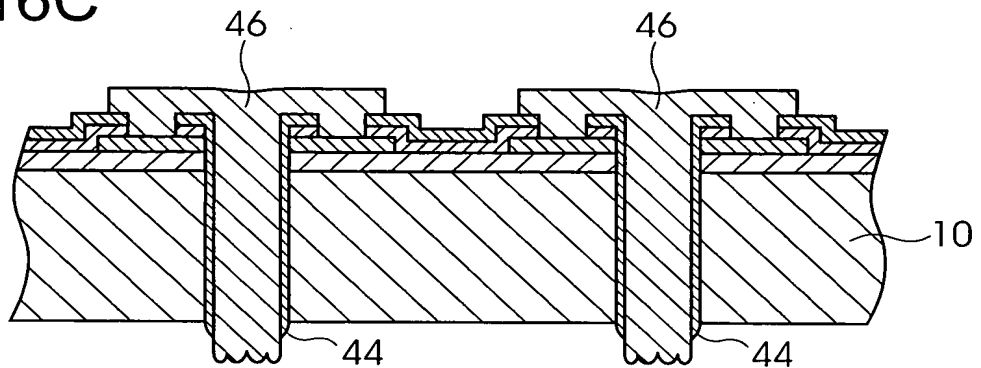
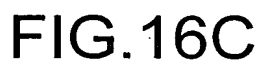


FIG.15B







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FIG.17

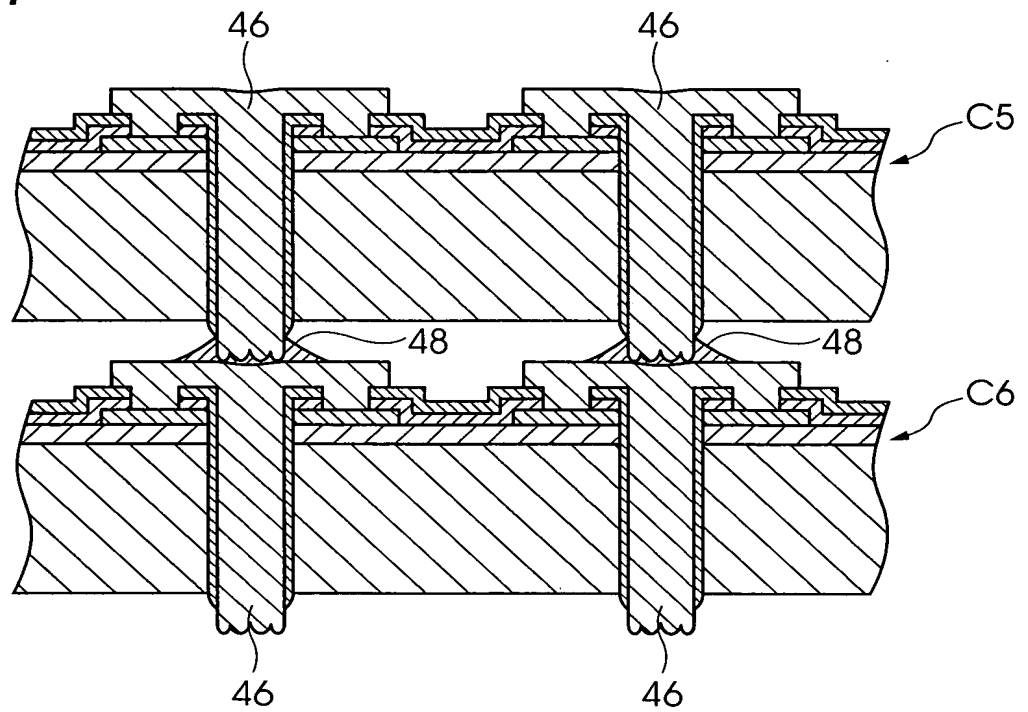


FIG.18

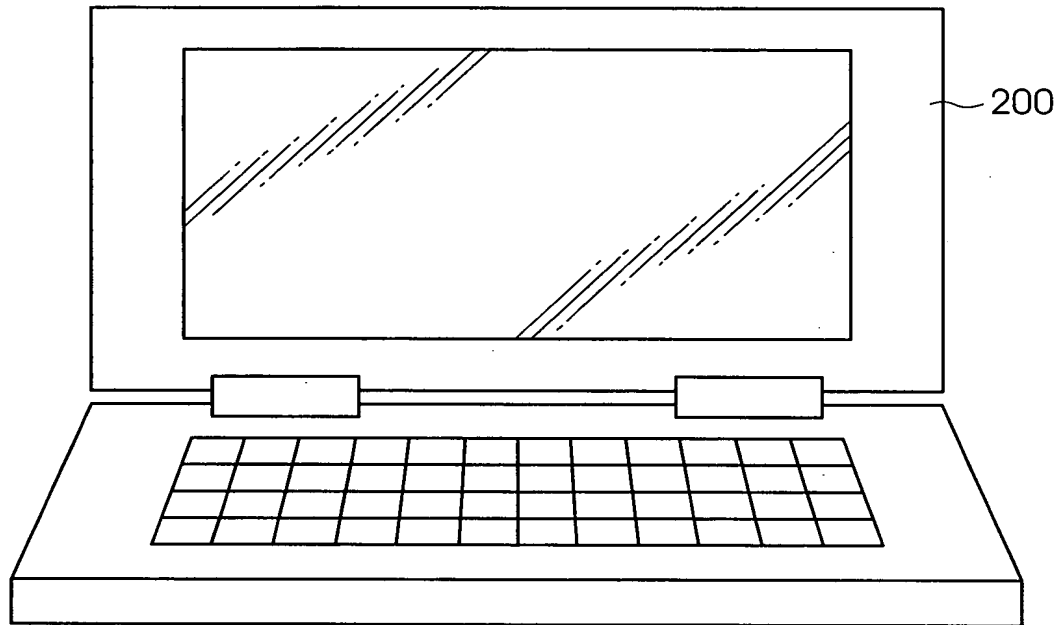


FIG.19

